THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte ASHOK KAPOOR

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Appeal No. 96-4080
Application 08/396,541[1]

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ON BRIEF

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Before HAIRSTON, FLEMING, and LALL, Administrative Patent Judges.

FLEMING, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 52, all of the claims pending in the present

[1] Application for patent filed March 1, 1996.

application. In an amendment filed after the final rejection entered by the Examiner, claims 2 and 28 have been canceled and claims 3, 13, 29 and 39 have been amended. Therefore, claims 1,

3 through 27 and 29 through 52 are properly before us for our consideration.

The invention relates to a microelectronic integrated circuit including a plurality of hexagonal CMOS "NAND" gate devices. On pages 4 through 7 of the specification, Appellant discloses that Figure 2 is an electrical schematic diagram illustrating Appellant's invention connected to provide a logical NAND function. In particular, Appellant discloses that gate device 30 includes a logical "ALL" element 133 having a hexagonal periphery 134 and a logical "ANY" element 233 having a hexagonal periphery 234. Appellant further discloses that in order to minimize the area required on the substrate 32 by the gate device 30, the logical "ALL" element 133 and the logical "ANY" element 233 are closely packed, with the peripheries 134 and 234 having a common edge. As illustrated in Figure 2, the edge 134-4 of the element 133 is

common with the edge 234-6 of the element 233.

The independent claim 1 is reproduced as follows:

1. A CMOS microelectronic device, comprising:
a hexagonal ANY element of a first conductivity type, having a first input and an output; and

a hexagonal ALL element of a second conductivity type which is opposite to said first conductivity type, having a first input and an output, in which:

said first inputs of the ANY and ALL elements are electrically interconnected, and said output of the ANY and ALL elements are electrically interconnected;

the ANY element has a periphery defined by a hexagon including first through sixth edges;

the ALL element has a periphery defined by a hexagon including first through sixth edges; and

one of said first through sixth edges of the ANY element is common with one of said first through sixth edges of the ALL element.

The Examiner relies on the following references:

Huang	5,198,881	Mar. 30, 1993
Bulucea	5,072,266	Dec. 10, 1991

Adel S. Sedra, Microelectronic Circuits, 1982, pp 734 and 801

Claims 1, 3 through 27 and 29 through 52 stand rejected under 35 U.S.C. § 103 as being unpatentable over Huang, Bulucea and Sedra.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the brief and answer for the

respective details thereof.

OPINION

We will not sustain the rejection of claims 1, 3 through 27 and 29 through 52 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed

invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied,*** 117 S.Ct. 80 (1996) ***citing W. L. Gore & Assocs., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

Appellant argues on pages 4 through 8 of the brief that Huang, Bulucea and Sedra, together or individually, fail to teach or suggest the claimed CMOS microelectronic device comprising a hexagonal ANY element of a first conductivity type, a hexagonal ALL element of a second conductivity type which is opposite to said first conductivity type in which one of the first through sixth edges of the ANY element is common with one of the first through sixth edges of the ALL element. We note that Appellant's independent claims 1 and 27 recite these limitations.

Upon a careful review of Huang, Bulucea and Sedra, we find that neither reference teaches a hexagonal ANY element of a first conductivity type, a hexagonal ALL element of a second conductivity type which is opposite to said first conductivity type in which one of the first through sixth edges of the ANY element is common with one of the first through sixth edges of the ALL element as recited in Appellant's claims. We agree with the Examiner that Huang teaches in column 6 a circuit

structure for pixel arrays which include CMOS gates and suggests alternative pixel shapes and geometries such as hexagonal arrays are suggested. In addition, we agree with the Examiner that Bulucea teaches a power MOSFET apparatus using a hexagon-shape trench in which the gate is positioned in order to suppress oxide and that Sedra teaches a CMOS NAND gate. However, neither Huang, Buluccea nor Sedra teaches or suggests arranging a hexagonal ANY element and a hexagonal ALL element of an opposite conductivity of the conductivity of the ANY element in which one of said first through sixth edges of the ANY element is common with one of the first through sixth edges of the ALL element as claimed by Appellant.

We are not inclined to dispense with proof by evidence when the proposition at issue is not supported by a teaching in a

prior art reference, common knowledge or capable of unquestion-able demonstration. Our reviewing court requires this evidence in order to establish a ***prima facie*** case. ***In re Knapp-Monarch Co.***, 296 F.2d 230, 232, 132 USPQ 6, 8 (CCPA

1961); ***In re Cofer***, 354 F.2d 664, 668, 148 USPQ 268, 271-72 (CCPA 1966).

Furthermore, the Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." ***Para-Ordnance Mfg.***, 73 F.3d at 1087, 37 USPQ2d at 1239, ***citing W. L. Gore***, 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13. We fail to find any suggestion in the prior art to modify Sedra's NAND gate to obtain Appellant's claimed invention.

Therefore, we have not sustained the rejection of claims 1, 3 through 27 and 29 through 52 under 35 U.S.C. § 103.

Accordingly, the Examiner's decision is reversed.

REVERSED

KENNETH W. HAIRSTON	)	
Administrative Patent Judge	)	
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	)	
	)	BOARD OF PATENT
MICHAEL R. FLEMING	)	
Administrative Patent Judge	)	APPEALS AND
	)	
	)	INTERFERENCES
	)	
PARSHOTAM S. LALL	)	
Administrative Patent Judge	)	

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Application 08/396,541

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